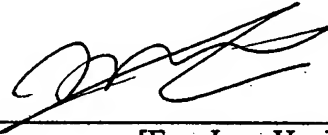


VERIFICATION OF TRANSLATION

I, Eun-Jung Han of 901 Seoyoung Bldg., 158-12, Samsung-dong, Kangnam-ku, Seoul,
135-090, Korea, declare that I have a thorough knowledge of the Korean and English languages,
and the writings contained in the following pages are correct English translation of the
specification and claims of Korean Patent Application No. 2002-0052660.

This 20th day of December, 2004

By:



[Eun-Jung Han]



**KOREAN INTELLECTUAL
PROPERTY OFFICE**

This is to certify that the following application annexed hereto
is a true copy from the records of the Korean Intellectual Property Office.

Application Number : 10-2002-0052660

Date of Application : September 14, 2002

Applicant(s) : LG. PHILIPS LCD CO., LTD.

May 22, 2003

COMMISSIONER

[BIBLIOGRAPHICAL DOCUMENTS]

[TITLE OF DOCUMENT] PATENT APPLICATION

[CLASSIFICATION] PATENT

[RECIPIENT] COMMISSIONER

[SUBMISSION DATE] 2002. 09. 03

[TITLE OF INVENTION IN KOREAN] 액정표시장치용 어레이기판과 제조방법

[TITLE OF INVENTION IN ENGLISH] Liquid Crystal Display and method for fabricating
of the same

[APPLICANT]

[NAME IN KOREAN] 엘지.필립스엘시디(주)

[NAME IN ENGLISH] LG. PHILIPS LCD CO., LTD.

[APPLICANT CORD] 1-1998-101865-5

[ATTORNEY]

[NAME] Jung, Won-Ki

[ATTORNEY CORD] 9-1998-000534-2

[ALL-INCLUSIVE AUTHORIZATION REGISTRATION NUMBER] 1999-001832-7

[INVENTOR]

[NAME IN KOREAN] 황용섭

[NAME IN ENGLISH] HWANG, YONG SUP

[IDENTIFICATION NO.] 741218-1674515

[ZIP CODE] 440-302

[ADDRESS] 207-804, Dongsin APT., Jeongja2-dong, Jangan-gu, Suwon-si,
Gyeonggi-do

[NATIONALITY] KR

[INVENTOR]

[NAME IN KOREAN] 채기성

[NAME IN ENGLISH] CHAE, GEE SUNG

[IDENTIFICATION NO.] 630125-1143617

[ZIP CODE] 406-130

[ADDRESS] 607-ho, 111-dong, Hanyang1-cha, Dongchun-dong, Yeonsu-gu,
Incheon

[NATIONALITY] KR

[INVENTOR]

[NAME IN KOREAN] 조규철

[NAME IN ENGLISH] JO, GYOO CHUL

[IDENTIFICATION NO.] 691010-1807618

[ZIP CODE] 435-040

[ADDRESS] 512-901, Gaya APT., 1155, Sanbon-dong, Gunpo-si, Gyeonggi-do

[NATIONALITY] KR

[PURPORT] We submit application as above under the article 42 of the Patent Law.

Attorney

Jung, Won-Ki (seal)

[FEES]

[BASIC APPLICATION FEE]	20 pages	29,000 won
[ADDITIONAL APPLICATION FEE]	17 pages	17,000 won
[PRIORITY FEE]	0 thing	0 won
[EXAMINATION REQUEST FEE]	0 claim	0 Won
[TOTAL]		46,000 Won

[ENCLOSED] 1. Abstract, Specification (with Drawings)_1 set

[DOCUMENT OF ABSTRACT]

[ABSTRACT]

The present invention relates to a liquid crystal display device, and more particularly, to an array substrate for a liquid crystal display device and a method of fabricating of the same.

In a first structure suggested by the present invention, a gate electrode is formed to have a double metal layer of copper (Cu) and metal, which has good adhesive characteristics to a substrate and etchant for which does not affect the substrate, such as molybdenum (Mo), chromium (Cr), tungsten (W) and nickel (Ni). A drain electrode is formed to have a double metal layer of copper (Cu) and metal, which does not react with copper due to etchant for patterning a transparent electrode, such as titanium (Ti), tantalum (Ta), molybdenum (Mo), chromium (Cr), tungsten (W) and nickel (Ni).

In a second structure suggested by the present invention, a passivation layer is further formed on a substantially entire surface of the substrate of the first structure as an insulation layer.

At this time, a gate electrode is formed to have a double metal layer of copper and metal, which has good adhesive characteristics to the substrate (Ti, Ta, Mo, Cr, W, and Ni), and a drain electrode is formed to have a double metal layer of copper and metal, which does not react with copper due to etchant for patterning a transparent electrode (Ti, Ta, Ti, Ta, Mo, Cr, W, and Ni).

If the gate and drain electrodes are formed to have a double metal layer including copper as stated above, delay in processes can be prevented, and driving characteristics of a thin film transistor can be improved to thereby increase a manufacturing yield.

[REPRESENTATIVE FIGURE]

FIG. 6e

[SPECIFICATIONS]

[NAME OF INVENTION]

Liquid Crystal Display and method for fabricating of the same

[BRIEF EXPLANATION OF FIGURES]

FIG. 1 is a plan view showing a part of an array substrate for a liquid crystal display device,

FIGS. 2a to 2f and FIGS. 3a to 3e are cross sectional views taken along II-II', III-III' and IV-IV' of FIG. 1 and illustrate manufacturing processes according to the related art,

FIG. 4 is an enlarged cross-sectional view of a portion D of FIG. 3e,

FIGS. 5a to 5d and FIGS. 6a to 6e are cross sectional views taken along II-II', III-III' and IV-IV' of FIG. 1 and illustrate manufacturing processes according to the present invention, and

FIG. 7 is a cross-sectional view of an array substrate for a liquid crystal display device according to a second embodiment of the present invention and taken along II-II', III-III' and IV-IV' of FIG. 1.

< Explanation of major parts in the figures >

121: substrate	131: gate electrode
133: gate line	135: gate pad electrode
137: gate insulation layer	139: active layer
141: ohmic contact layer	149: source electrode
151: drain electrode	153: data line

155: data pad electrode

157: source drain metal layer

159: passivation film

169: pixel electrode

171: gate pad electrode terminal

173: data pad electrode terminal.

[DETAILED DESCRIPTION OF INVENTION]

[OBJECT OF INVENTION]

[TECHNICAL FIELD OF THE INVENTION AND PRIOR ART OF THE FIELD]

The present invention relates to a liquid crystal display device, and more particularly, to an array substrate for a liquid crystal display device, which includes a gate electrode and source and drain electrodes of a double-layered metal structure including copper, and a method of fabricating the same.

FIG 1 is an enlarged plan view of a part of an array substrate for a liquid crystal display device.

On a substrate 21, thin film transistors T, as switching elements, are arranged in a matrix type, and gate lines 33 and data lines 53 are formed intersecting the thin film transistors T.

A gate pad electrode 35 is formed at the end of each gate line 33, and this gate pad electrode 35 has a wider width than the gate line 33.

A data pad electrode 55 is formed at the end of each data line 53, and also has a wider width than the data line 53.

The gate pad electrode 35 and the data pad electrode 55 contact a gate pad electrode terminal 71 and a data pad electrode terminal 73, respectively, which are transparent and directly receive signals from the outside.

At this time, a region defined by crossing each gate line 33 and each data line 53 is referred to as a pixel region P.

A storage capacitor C is formed over a part of each gate line 33, and the storage capacitor C is electrically connected in parallel with a transparent pixel electrode 69 formed in the pixel region P.

Each thin film transistor T includes a gate electrode 31, a source electrode 49, a drain electrode 51, and an active layer 39 formed over the gate electrode 31.

In the above-mentioned structure, the capacitor C includes a part of the gate line 33 as a first electrode and a source-drain metal layer 57 as a second electrode. The source-drain metal layer 57 is formed over the part of the gate line 33 and formed of the same material in the same layer as the source and drain electrodes 49 and 51. The source-drain metal layer 57 is connected to the pixel electrode 69 through a contact hole 63.

Of the above-mentioned structure, the gate electrode 31, the gate line 33 and the gate pad electrode 35 are formed of aluminum (Al) (or aluminum alloy) of low resistive metal in order to prevent signal delay. Generally, the gate electrode 31, the gate line 33 and the gate pad electrode 35 are formed by depositing a double layer of aluminum (or aluminum alloy) and an additional metal layer so as to compensate weakness of aluminum (or aluminum alloy) during the process.

Furthermore, the drain electrode 51, the data line 53 and the data pad electrode 55 can be formed of aluminum. At this time, additional metal layers are further formed over and under aluminum (or aluminum alloy).

Hereinafter, fabrication process steps of an array substrate for a liquid crystal display device according to a related art will be explained in detail with reference to FIGS. 2a to 2d and FIGS. 3a to 3e.

First, FIGS. 2a to 2d are cross sectional views illustrating a process of forming a gate electrode, a gate line and a gate pad electrode according to the related art.

In general, a gate line, a gate electrode and a gate pad electrode are formed to have a double metal layer including aluminum. Aluminum (Al) has a low resistance. However, because aluminum (Al) is delicate to acidity and may result in line defects by a formation of a hillock during a following high temperature process, so molybdenum (Mo) or chromium (Cr) having high corrosion resistance is formed on the aluminum.

Hereinafter, the process of forming the gate electrode, the gate line and the gate pad electrode will be explained.

As shown in FIG. 2a, aluminum (Al) or aluminum alloy (AlNd) is deposited on a substrate 21, thereby forming a first metal layer 23a, and then molybdenum (Mo) is deposited on the first metal layer 23a, thereby forming a second metal layer 23b.

Sequentially, photoresist (hereinafter referred to as "PR") is coated on the second metal layer 23b to thereby form a PR layer 25.

Next, a mask M, which includes light-transmitting portions A and light-shielding portions B, is disposed over the PR layer 25, and then a light exposure is performed to the PR layer 25 by irradiating light through the mask M.

Sequentially, the light-exposed PR layer 25 is developed.

As shown in FIG. 2b, the second metal layer 23b is exposed between the PR layers 27 remaining after developing.

At this time, the remaining PR layers 27 are backed, and thus the PR layers 27 have a semicircular shape.

As shown in FIG. 2c, the first metal layer 23a and the underlay second metal layer 23b exposed between the remaining PR layers 27 are wet-etched. Since patterned first metal

layer 23a of aluminum (Al) or aluminum alloy is etched faster than patterned second metal layer 23b of molybdenum (Mo), the first metal layer 29a and the second metal layer 29b have an overhang shape.

Since this overhang shape causes the later-formed insulator (not shown) to have deposition defects, a process for sequentially tapering sides of the patterned first metal layer 29a and the patterned second metal layer 29b is needed.

As shown in FIG. 2d, therefore, a dry etching method is used to etch both sides of the remaining PR layers 27 (circumference in plane) and the first and second metal layers 29a and 29b under them. At this time, the remaining PR layers 27 are removed maintaining shapes thereof.

If done like this, as stated above, the first and second metal layers 29a and 29b have sides of a sequentially tapered shape.

After the dry etching process is completed, the remaining PR layers 27 are removed.

As shown in FIG. 2e, as a result, the gate electrode 31 and the gate line 33, which is connected to the gate electrode 31 and has a gate pad electrode 35 at one end thereof, can be formed to have a double metal layer of aluminum (or aluminum alloy)/molybdenum (Al(AlNd)/Mo). As described in FIG. 1, the gate electrode 31 extends from the gate line 33 and the gate pad electrode 35 is at the end of the gate line 33.

Hereinafter, FIGS. 3a to 3e show processes following the processes of FIGS. 2a to 2e.

As shown in FIG. 3a, a gate insulation layer 37 is formed as a first insulation layer by depositing one selected from an inorganic insulating material group including silicon nitride (SiN_x) and silicon oxide (SiO_2) on an entire surface of the substrate 21, where the gate electrode 31, the gate line 33 and the gate pad electrode 35 are formed.

Subsequently, amorphous silicon (a-Si:H) and impurity-doped amorphous silicon (n^+

a-Si:H) are deposited on the gate insulation layer 37 over the gate electrode 31 and then patterned to form an active layer 39 and an ohmic contact layer 41.

Next, as shown in FIG. 3b, third, fourth and fifth metal layers 43, 45 and 47 are formed sequentially by depositing molybdenum (Mo), aluminum (Al) and molybdenum (Mo) on an entire surface of the substrate 21, where the ohmic contact layer 41 is formed.

Next, as shown in FIG. 3c, the third, fourth and fifth metal layers are simultaneously patterned, and thus a source electrode 49, a drain electrode 51 and a data line 53 are formed. The source electrode 49 and the drain electrode 51 include a triple-layered structure of molybdenum/aluminum/molybdenum (Mo/Al/Mo). The source electrode 49 and the drain electrode 51 are spaced apart from each other and contact the ohmic contact layer 41. The data line 53 is connected to the source electrode 49 and includes a data pad 55 at one end thereof.

At the same time, a source drain metal layer 57 of an island shape is formed over a part of the gate line 33.

If a large size substrate is fabricated to include the source and drain electrodes 49 and 51 and the data line 53 formed into a single layer of molybdenum (Mo) or chromium (Cr), which has high resistance, it is hard to obtain an uniform image quality all over the liquid crystal panel due to signal delay.

In contrast, the lower resistance the source and drain electrodes 49 and 51 and the data line 53 has, the better the signal flows, and thus the array substrate can be fabricated in large size.

Therefore, to solve this, it is necessary that the source and drain electrodes 49 and 51 and the data line 45 are formed to have low resistance.

By the way, of the molybdenum layers of the low resistant line, which are formed

over and under the aluminum layer, respectively, the lower molybdenum layer prevents a spiking phenomenon where the aluminum layer, the second metal layer, penetrates into the active layer 39 or the ohmic contact layer 41. The upper molybdenum layer reduces a contact resistance between the aluminum layer and a later-formed transparent electrode.

On the ground of such purposes, the source and drain electrodes 49 and 51 and the data line 53 are formed to have the triple-layered structure (Mo/Al/Mo).

In succession to the above-mentioned process, the ohmic contact layer 41 exposed between the source electrode 49 and the drain electrode 51 is etched to thereby expose the active layer 39.

As shown in FIG. 3d, a passivation film 59 is formed as a second insulation layer by depositing an insulating material on an entire surface of the substrate 21, where the source and drain electrodes 49 and 51 are formed.

The passivation film 59 is etched to thereby form a drain contact hole 61 that exposes a part of the drain electrode 51, a storage contact hole 63 that exposes a part of the source drain metal layer, a gate pad electrode contact hole 65 that exposes the gate pad electrode 35, and a data pad contact hole 67 that exposes the data pad electrode 37.

As shown in FIG. 3e, a transparent pixel electrode 69 is formed by depositing one selected from a transparent conductive metal group including indium-tin-oxide (ITO) and indium-zinc-oxide (IZO) on an entire surface of the substrate 21, where the passivation film 59, and then patterning it. The pixel electrode 69 contacts the drain electrode 51 and the source-drain metal layer 47.

Simultaneously, a gate pad electrode terminal 71 contacting the gate pad electrode 35 and a data pad electrode terminal 73 contacting the data pad electrode 55 are formed.

The array substrate of the related art can be manufactured through the above-

mentioned processes.

Although the processes may include five mask processes, the processes may be delayed because the gate electrode and the gate line need to get through the double-etching process: the wet etching process and the dry etching process.

In addition, among the processes of the related art, the source and drain electrodes 49 and 51, the data line 53 and the data pad electrode 55 are formed by simultaneously etching the triple-layered metal using a mixed acid solution, and the electrochemical reaction (a Galvanic Reaction) will be caused by the etching solution during this etching process. At this time, as the molybdenum (Mo) becomes thicker, it is much difficult to overcome the electrochemical reaction.

Especially, the lower molybdenum layer is over-etched due to the electrochemical reaction, and thus the aluminum layer collapses and contacts the active layer during the process for forming the passivation layer.

At this time, the aluminum layer and the active layer react with each other and cause the increase of the leakage current to thereby deteriorate the operating characteristics of the device.

Hereinafter, explanations will be given with reference to FIG. 4. FIG. 4 is an enlarged cross-sectional view of a portion D of FIG. 3e.

As shown in the figure, molybdenum (Mo) layers formed over and under the aluminum layer 45 are over-etched.

This phenomenon causes that the passivation film is not formed properly due to reverse taper E of the aluminum when the passivation film 55 is formed on an entire surface of the substrate, where the source and drain electrodes 49 and 51 of FIG. 3e, the data line 53 of FIG. 3e and the data pad electrode 55 of FIG. 3e are formed.

Additionally, the aluminum layer is pressed by the passivation layer 59 formed thereon and contacts the active layer 39 or the ohmic contact layer 41. In this case, the leakage current increases due to mutual diffusion action, and thus operation of the device (thin film transistor) is deteriorated.

[TECHNICAL SUBJECT OF INVENTION]

To solve the above-mentioned problems, when the gate electrode and the source and drain electrodes are formed to have a double metal layer including copper and a buffer metal layer.

At this time, the buffer metal layer, which is used as the gate electrode with copper, should have good adhesive characteristics to a substrate, and etchant for the buffer metal layer may not damage the substrate.

Moreover, the buffer metal layer, which is used as the source and drain electrodes with copper, may not react with an active layer and an ohmic contact layer and may not cause the electrochemical reaction due to the etching solution of the transparent pixel electrode (ITO electrode).

Like this, if the gate and drain electrodes are formed to have a double metal layer including copper, two etching processes for forming the gate electrode are not necessary, and the leakage current problem, which may occur when the source and drain electrodes are formed to have the triple-layered structure including aluminum, may be solved.

[CONSTRUCTION OF INVENTION]

An array substrate for a liquid crystal display device for achieving the above-mentioned objects includes a gate electrode, a gate line and a gate pad electrode on a substrate,

the gate electrode composed of a double layer of copper and a first metal buffer layer, the gate line connected to the gate electrode, the gate pad electrode extending from the gate line; a first insulation layer on the gate electrode, the gate line and the gate pad electrode; an active layer and an ohmic contact layer laminated on the first insulation layer over the gate electrode; source and drain electrodes contacting the ohmic contact layer and composed of a double layer of copper and a second metal buffer layer, a data line connected to the source electrode, and a data pad electrode extending from the data line; a passivation film on an entire surface of the substrate, where the source electrode, the drain electrode, and the data line are formed, and exposing parts of the drain electrode, the gate pad electrode and the data pad electrode; and a transparent pixel electrode contacting the exposed drain electrode, a transparent gate pad electrode terminal contacting the gate pad electrode, and a transparent data pad electrode terminal contacting the data pad electrode.

The first metal buffer layer is formed of a material that has good adhesive characteristics to the substrate and a patterning solution for which does not damage the substrate. These materials are chromium (Cr), molybdenum (Mo), nickel (Ni), tungsten (W), and so on.

The second metal buffer layer is formed of a material that does not contact and react with the active layer and the ohmic contact layer and that does not have an electrochemical reaction with the copper due to an etching solution for patterning the pixel electrode. These materials are tantalum (Ta), titanium (Ti), chromium (Cr), molybdenum (Mo), nickel (Ni), tungsten (W), and so on.

A source drain metal layer of an island shape is further formed of a same material and in a same layer as the source and drain electrodes over a part of the gate line, and the source-drain metal layer contacts the pixel electrode through a contact hole that is formed by

etching the passivation film.

A passivation layer is further formed on an entire surface of the substrate under the gate electrode, the gate line and the gate pad electrode.

The passivation layer is formed of one selected from an inorganic insulating material group including silicon nitride (SiN_x) and silicon oxide (SiO_2) or one selected from an organic insulating material group including benzocyclobutene (BCB) and acryl resin.

In the case that the passivation layer is further formed, the first metal buffer layer is formed of a material that has a good adhesive characteristic to the substrate, and these materials are tantalum (Ta), titanium (Ti), chromium (Cr), molybdenum (Mo), nickel (Ni), tungsten (W), and so on.

A method of manufacturing an array substrate for a liquid crystal display device according to the special feature of the present invention includes forming a gate electrode, a gate line and a gate pad electrode on a substrate, the gate electrode composed of a double layer of copper and a first metal buffer layer, the gate line connected to the gate electrode, the gate pad electrode extending from the gate line; forming a first insulation layer on the gate electrode, the gate line and the gate pad electrode; forming an active layer and an ohmic contact layer on the first insulation layer over the gate electrode; forming source and drain electrodes contacting the ohmic contact layer and of a double layer of copper and a second metal buffer layer, a data line connected to the source electrode, and a data pad electrode extending from the data line; forming a passivation film on an entire surface of the substrate, where the source electrode, the drain electrode, and the data line are formed, and exposing parts of the drain electrode, the gate pad electrode and the data pad electrode; and forming a transparent pixel electrode contacting the exposed drain electrode, a transparent gate pad electrode terminal contacting the gate pad electrode, and a transparent data pad electrode

terminal contacting the data pad electrode.

Hereinafter, exemplary embodiments according to the present invention will be explained with reference to drawings.

-- first embodiment --

In a first embodiment of the present invention, a gate electrode and source and drain electrodes are formed to have a double metal layer including copper.

Hereinafter, a process of manufacturing an array substrate according to the present invention will be explained with reference to FIGS. 5a to 5d and FIGS. 6a to 6e. (Because a plan view of the present invention is the same as the plan view of the related art, the plan view of the related art may be used, and references for the same parts may be designated by adding 100 to the numbers of the related art.

FIGS. 5a to 5d are cross sectional views illustrating a process of forming a gate electrode, a gate line and a gate pad electrode according to the present invention.

First, a first metal layer 123a is formed on a substrate 121 by depositing one selected from a conductive metal group including molybdenum (Mo), chromium (Cr), tungsten (W), nickel (Ni) and alloys thereof, and then a second metal layer 123b is formed on the first metal layer 123a by depositing copper (Cu).

At this time, since copper does not have good adhesive characteristics to a glass substrate, a metal layer is further formed under copper in order to solve this.

Sequentially, photoresist (hereinafter referred to as "PR") is coated on the second metal layer 123b to thereby form a PR layer 125.

Next, a mask M having light-transmitting portions A and light-shielding portions B is disposed over the PR layer 125, and then a light exposure is performed to the PR layer 125 by

irradiating light through the mask M.

Sequentially, the light-exposed PR layer 125 is developed.

As shown in FIG. 5b, the second metal layer 123b is exposed between the PR layers 127 remaining after developing.

At this time, the remaining PR layers 127 are backed, and thus the PR layers 127 have a semicircular shape.

As shown in FIG. 5c, the second metal layer 125b and the underlay first metal layer 125a exposed between the remaining PR layers 127 are wet-etched, and a patterned first metal layer 129a of the copper (Cu) layer and a patterned second metal layer 129a have sides sequentially tapered.

In succession, the remaining PR layers are removed, and as shown in FIG. 5d, a gate electrode 131, which includes a double layer of copper/buffer metal layer (Cu/one selected among Cr, Mo, W and Ni), and a gate line 133, which is connected to the gate electrode 131 and has a gate pad electrode 135 at one end thereof, can be formed.

Tantalum (Ta) and titanium (Ti) may be further included as the buffer metal layer, and they are not used because an etching solution for etching tantalum (Ta) and titanium (Ti) can damage a glass substrate.

Following the process for forming the gate electrode, the gate line and the gate pad, a process of the array substrate for the liquid crystal display device according to the present invention will be explained with reference to FIGS. 6a to 6e.

As shown in FIG. 6a, a gate insulation layer 137 is formed on an entire surface of the substrate 121, where the gate electrode 131, the gate line 133, and so on are formed, as a first insulation layer.

The gate insulation layer 137 is formed by depositing one selected from an inorganic

insulating group including silicon nitride (SiN_x) and silicon oxide (SiO_2).

Next, an active layer 139 and an ohmic contact layer 141 are formed on the gate insulation layer 137 over the gate electrode 131 in an island shape.

The active layer 139 is generally formed of pure amorphous silicon (a-Si:H), and the ohmic contact layer 141 is formed of impurity-doped amorphous silicon (n+a-Si:H).

Next, as shown in FIG. 6b, a first metal layer 143 is formed on an entire surface of the substrate 121, where the ohmic contact layer 141 is formed, by depositing one selected from a conductive metal group including tantalum (Ta), titanium (Ti), molybdenum (Mo), chromium (Cr), nickel (Ni), and so on, and a second metal layer 145 is formed on the first metal layer 143 by depositing copper (Cu).

At this time, the first metal layer 143 can prevent the second metal layer 145 of the copper layer and the semiconductor layer from directly contacting and reacting with each other.

Next, as shown in FIG. 6c, the first metal layer and the second metal layer are wet-etched, thereby forming a source electrode 149 of a double metal layer including copper, and a drain electrode 151 spaced apart from this, and a data line 153 connected to the source electrode 149 and including a data pad 155 at one end thereof.

Simultaneously, a source-drain metal layer 157 of an island shape is formed over a part of the gate line 133.

Sequentially, the ohmic contact layer 141 exposed in a portion between the source electrode 149 and the drain electrode 151 spaced apart is etched, and thus the active layer 139 thereunder is exposed.

In the process of forming the source and drain electrodes, if the first metal layer 143 of FIG. 6b is formed of molybdenum (Mo), electrochemical reaction may occur between the

copper (Cu) and molybdenum (Mo) layers due to an etching solution for etching the first metal layer 143 of FIG. 6b and the second metal layer 145 of FIG. 6b according to circumstances.

In this case, the copper (Cu) and the molybdenum (Mo) cannot be simultaneously used depending on the etching solution.

Next, as shown in FIG. 6d, a passivation film 159 is formed on an entire surface of the substrate 121, where the source and drain electrodes 149 and 151 are formed, by depositing one selected from an inorganic insulating material group including silicon nitride (SiO_2) and silicon oxide (SiN_x) or by coating one selected from an organic insulating material group including benzocyclobutene (BCB) and acryl resin.

The passivation film 159 is patterned, thereby forming a drain contact hole 161 exposing a part of the drain electrode 151, a storage contact hole 163 exposing the source-drain metal layer 157, a gate pad electrode contact hole 165 exposing a part of the gate pad electrode 135, a data pad contact hole 167 exposing the gate pad electrode 137.

Next, as shown in FIG. 6e, one selected from a transparent conductive metal group including indium-tin-oxide (ITO) and indium-zinc-oxide (IZO) is deposited on the passivation film 159, thereby forming a pixel electrode 169 contacting the drain electrode 151 and the source-drain metal layer 157, a gate pad electrode terminal 171 contacting the gate pad electrode 135, and a data pad electrode terminal 173 contacting the data pad electrode 137.

The array substrate according to the first embodiment of the present invention may be manufactured through the above-mentioned processes.

As stated above, if copper having low resistivity characteristics is used when the gate electrode and the source and drain electrode are formed, the manufacturing time can be shortened, and driving characteristics of the device may be improved.

In the first embodiment, the defects of copper are compensated by using the double metal layer of the copper and the metal buffer layer. That is, the copper has poor characteristics in contact with the glass substrate, and the leakage current increases due to mutual diffusion action when the copper contacts the ohmic contact layer. To prevent this, a metal, such as molybdenum (Mo), chromium (Cr), tungsten (W), nickel (Ni), and so forth, is used as the buffer layer.

At this time, in the case that copper is used as the gate metal, tantalum (Ta) and titanium (Ti) cannot be used as the metal buffer layer as stated above, and a method for solving this hereinafter will be explained through a second embodiment.

-- second embodiment --

A special feature of a second embodiment of the present invention is to form a passivation layer on an entire surface of a substrate as an insulation layer before forming the gate electrode.

Explanation will be followed with reference to FIG. 7.

FIG. 7 is a cross-sectional view of an array substrate for a liquid crystal display device according to a second embodiment of the present invention and taken along II-II', III-III' and IV-IV' of FIG. 1.

As shown in the figure, a passivation layer 130 is formed on a substrate 121, and a gate electrode 131 of a double metal layer composed of copper (Cu) and a buffer metal layer (one selected among Ti, Ta, W, Cr, Ni and Mo) and a gate line 133 connected to this and having a gate pad electrode 135 at one end thereof are formed.

A gate insulation layer 137 is formed on an entire surface of the substrate 121 including the gate electrode 131 and the gate line 133.

An active layer 139 and an ohmic contact layer 141 are formed on the gate insulation layer 137 over the gate electrode 131, and source and drain electrodes 149 and 151, which contact the ohmic contact layer 141, are spaced apart from each other, and are a double layer of copper (Cu) and a buffer metal layer (one selected among Ti, Ta, W, Cr, Ni and Mo), and a data line 153, which is connected to the source electrode 149 and includes a data pad 155 at one end thereof, are formed.

At this time, a source drain metal layer 157 is formed of the same material and in the same layer as the source and drain electrodes 149 and 151 over a part of the gate line 133.

A passivation film 159 exposing a part of the drain electrode 151 is formed on an entire surface of the substrate 121, where the source and drain electrodes 149 and 151 are formed.

A pixel electrode 169 contacting the drain electrode 151, a gate pad electrode electrode terminal 171 contacting the gate pad electrode 135, and a data pad electrode terminal 173 contacting the data pad electrode 155 are formed on the passivation film 159.

In the above-mentioned structure, the passivation layer 130 is formed by depositing or coating one selected from an inorganic insulating material group including silicon nitride (SiN_x) or silicon oxide (SiO_2) and one selected from an organic insulating material group including benzocyclobutene (BCB) and acryl resin.

In addition to molybdenum (Mo), chromium (Cr), tungsten (W) and nickel (Ni), titanium (Ti) and tantalum (Ta) can be further used as the metal buffer layer, which is formed for the gate electrode 131 with copper, owing to the passivation layer 130.

That is, because the etching solution for etching the titanium (Ti) and tantalum (Ta) does not touch the substrate 121 by forming the passivation layer 130 on the substrate 121, they can be used.

The array substrate for the liquid crystal display device according to the second embodiment of the present invention can be manufactured with the above-mentioned structure.

[EFFECT OF INVENTION]

If an array substrate for a liquid crystal display device is manufactured according to the present invention, first, there is an effect that the manufacturing time can be reduced because a double metal layer including copper are etched at once by the same etching solution

Second, there is an effect that driving characteristics of a thin film transistor can be improved because a metal for forming a drain electrode does not react with an active layer thereunder.

Third, there is an effect that a large size liquid crystal display device can be manufacture because copper of low resistance is used as a gate material and a source and drain material.

[RANGE OF CLAIMS]

[CLAIM 1]

An array substrate for a liquid crystal display device comprising:

a gate electrode, a gate line and a gate pad electrode on a substrate, the gate electrode composed of a double layer of copper and a first metal buffer layer, the gate line connected to the gate electrode, the gate pad electrode extending from the gate line;

a first insulation layer on the gate electrode, the gate line and the gate pad electrode;

an active layer and an ohmic contact layer laminated on the first insulation layer over the gate electrode;

source and drain electrodes contacting the ohmic contact layer and composed of a double layer of copper and a second metal buffer layer, a data line connected to the source electrode, and a data pad electrode extending from the data line;

a passivation film on an entire surface of the substrate, where the source electrode, the drain electrode, and the data line are formed, and exposing parts of the drain electrode, the gate pad electrode and the data pad electrode; and

a transparent pixel electrode contacting the exposed drain electrode, a transparent gate pad electrode terminal contacting the gate pad electrode, and a transparent data pad electrode terminal contacting the data pad electrode.

[CLAIM 2]

The array substrate for the liquid crystal display device according to claim 1,

wherein the first metal buffer layer is formed of a material that has good adhesive characteristics to the substrate and a patterning solution for which does not damage the substrate.

[CLAIM 3]

The array substrate for the liquid crystal display device according to claim 2,
wherein the material for forming the first metal buffer layer is one selected from a metal group composed of chromium (Cr), molybdenum (Mo), nickel (Ni) and tungsten (W).

[CLAIM 4]

The array substrate for the liquid crystal display device according to claim 1,
wherein the second metal buffer layer is formed of a material that does not contact and react with the active layer and the ohmic contact layer and that does not have an electrochemical reaction with the copper due to an etching solution for patterning the pixel electrode.

[CLAIM 5]

The array substrate for the liquid crystal display device according to claim 4,

wherein the material for forming the second metal layer is one selected from a metal group composed of tantalum (Ta), titanium (Ti), chromium (Cr), molybdenum (Mo), nickel (Ni) and tungsten (W).

[CLAIM 6]

The array substrate for the liquid crystal display device according to claim 1,

further comprising a source drain metal layer that is formed of a same material and in a same layer as the source and drain electrodes over a part of the gate line and that is an island shape.

[CLAIM 7]

The array substrate for the liquid crystal display device according to claim 6,

wherein the source-drain metal layer contacts the pixel electrode through a contact hole that is formed by etching the passivation film.

[CLAIM 8]

The array substrate for the liquid crystal display device according to claim 1,

further comprising a passivation layer on an entire surface of the substrate under the gate electrode, the gate line and the gate pad electrode.

[CLAIM 9]

The array substrate for the liquid crystal display device according to claim 8,

wherein the passivation layer is formed of one selected from an inorganic insulating material group including silicon nitride (SiN_x) and silicon oxide (SiO_2) or one selected from an organic insulating material group including benzocyclobutene (BCB) and acryl resin.

[CLAIM 10]

The array substrate for the liquid crystal display device according to claim 8,

wherein the first metal buffer layer is formed of a material that has a good adhesive characteristic to the substrate.

[CLAIM 11]

The array substrate for the liquid crystal display device according to claim 10,

wherein the material for forming the second metal layer is one selected from a metal group composed of tantalum (Ta), titanium (Ti), chromium (Cr), molybdenum (Mo), nickel (Ni) and tungsten (W).

[CLAIM 12]

An array substrate for a liquid crystal display device comprising:

forming a gate electrode, a gate line and a gate pad electrode on a substrate, the gate electrode composed of a double layer of copper and a first metal buffer layer, the gate line connected to the gate electrode, the gate pad electrode extending from the gate line;

forming a first insulation layer on the gate electrode, the gate line and the gate pad electrode;

forming an active layer and an ohmic contact layer on the first insulation layer over the gate electrode;

forming source and drain electrodes contacting the ohmic contact layer and of a double layer of copper and a second metal buffer layer, a data line connected to the source electrode, and a data pad electrode extending from the data line;

forming a passivation film on an entire surface of the substrate, where the source electrode, the drain electrode, and the data line are formed, and exposing parts of the drain electrode, the gate pad electrode and the data pad electrode; and

forming a transparent pixel electrode contacting the exposed drain electrode, a transparent gate pad electrode terminal contacting the gate pad electrode, and a transparent data pad electrode terminal contacting the data pad electrode.

[CLAIM 13]

The method of manufacturing the array substrate for the liquid crystal display device according to claim 12,

wherein the first metal buffer layer is formed of a material that has good adhesive characteristics to the substrate and a patterning solution for which does not damage the substrate.

[CLAIM 14]

The method of manufacturing the array substrate for the liquid crystal display device according to claim 13,

wherein the material for forming the first metal buffer layer is one selected from a metal group composed of chromium (Cr), molybdenum (Mo), nickel (Ni) and tungsten (W).

[CLAIM 15]

The method of manufacturing the array substrate for the liquid crystal display device according to claim 12,

wherein the second metal buffer layer is formed of a material that does not contact and react with the active layer and the ohmic contact layer and that does not have an electrochemical reaction with the copper due to an etching solution for patterning the pixel electrode.

[CLAIM 16]

The method of manufacturing the array substrate for the liquid crystal display device according to claim 15,

wherein the material for forming the second metal layer is one selected from a metal group composed of tantalum (Ta), titanium (Ti), chromium (Cr), molybdenum (Mo), nickel (Ni) and tungsten (W).

[CLAIM 17]

The method of manufacturing the array substrate for the liquid crystal display device according to claim 12,

further comprising forming a source drain metal layer that is made of a same material and in a same layer as the source and drain electrodes over a part of the gate line and that is an island.

[CLAIM 18]

The method of manufacturing the array substrate for the liquid crystal display device according to claim 17,

further comprising contacting the source-drain metal layer with the pixel electrode through a contact hole that is formed by etching the passivation film.

[CLAIM 19]

The method of manufacturing the array substrate for the liquid crystal display device according to claim 12,

further comprising forming a passivation layer on an entire surface of the substrate under the gate electrode, the gate line and the gate pad electrode.

[CLAIM 20]

The method of manufacturing the array substrate for the liquid crystal display device according to claim 19,

wherein the passivation layer is formed of one selected from an inorganic insulating material group including silicon nitride (SiN_x) and silicon oxide (SiO_2) or one selected from an organic insulating material group including benzocyclobutene (BCB) and acryl resin.

[CLAIM 21]

The method of manufacturing the array substrate for the liquid crystal display device according to claim 19,

wherein the first metal buffer layer is formed of a material that has a good adhesive characteristic to the substrate.

[CLAIM 22]

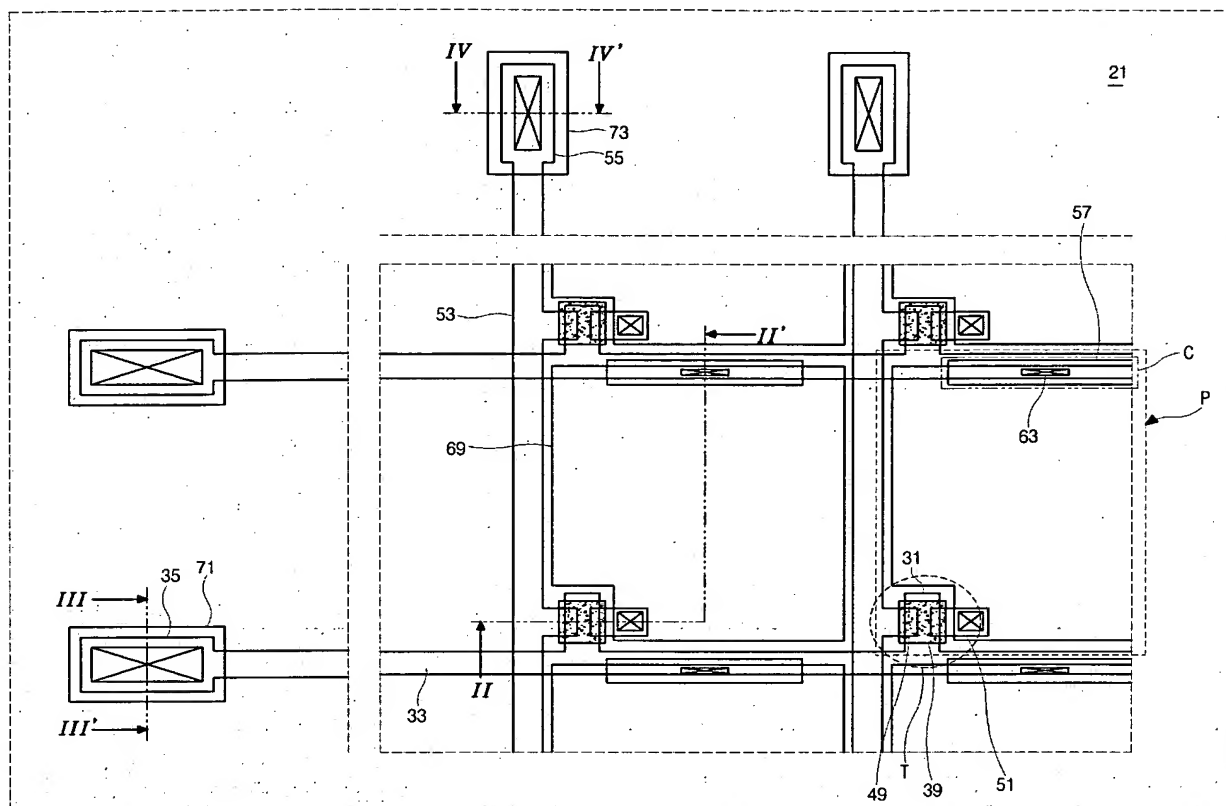
The method of manufacturing the array substrate for the liquid crystal display device according to claim 21,

wherein the material for forming the second metal layer is one selected from a metal group composed of tantalum (Ta), titanium (Ti), chromium (Cr), molybdenum (Mo), nickel (Ni) and tungsten (W).

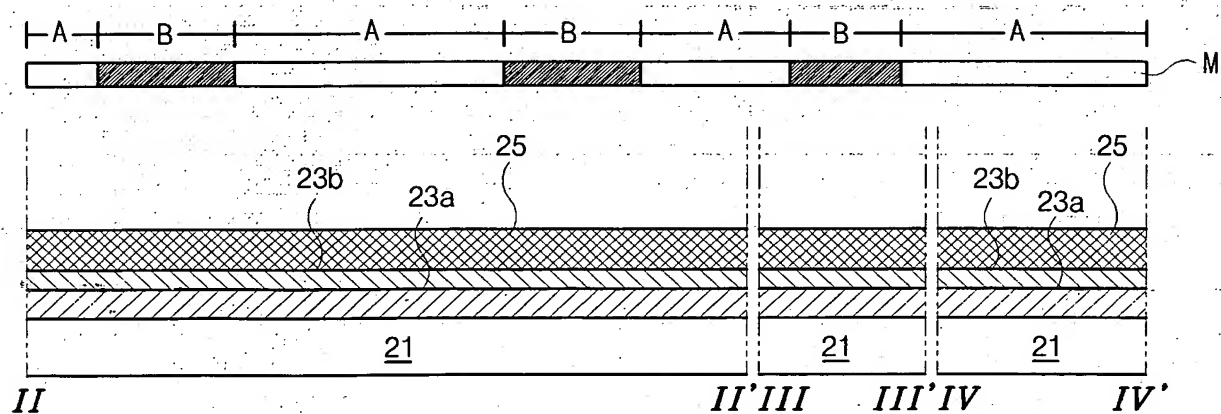


[DRAWINGS]

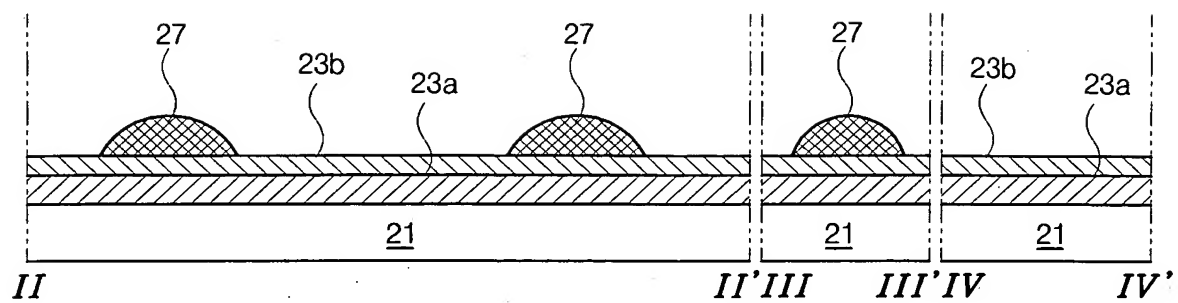
[Fig. 1]



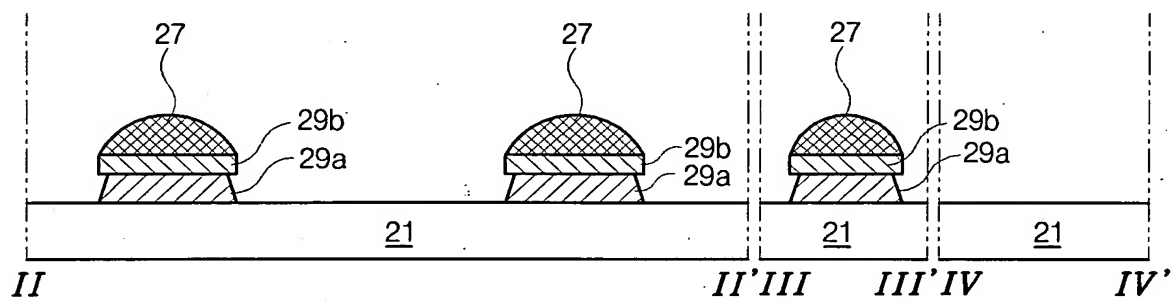
[Fig. 2a]



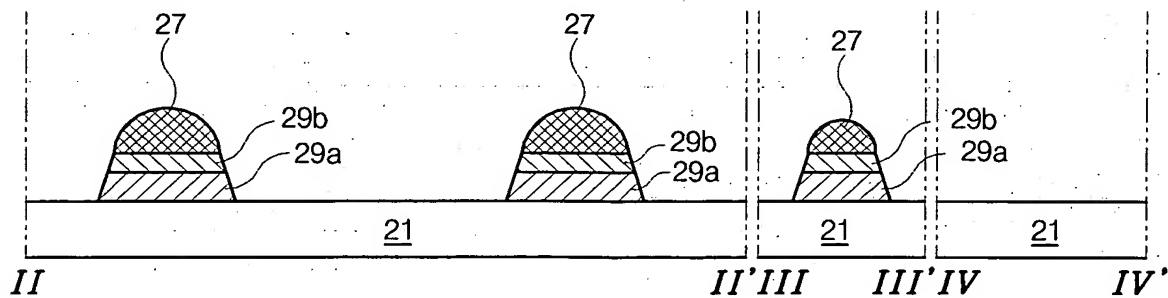
[Fig. 2b]



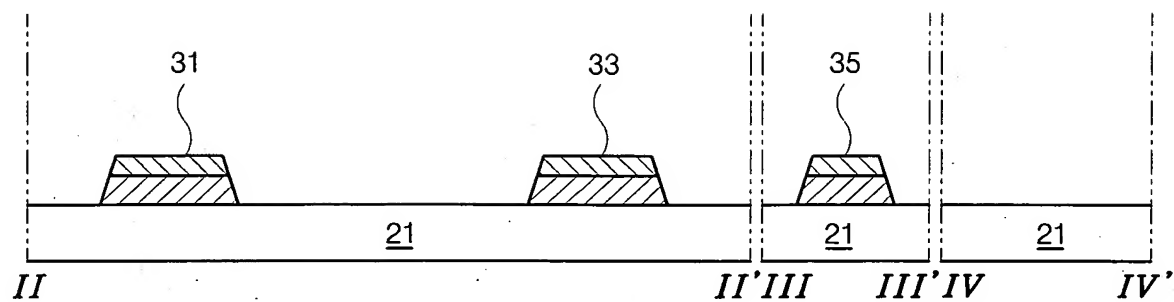
[Fig. 2c]



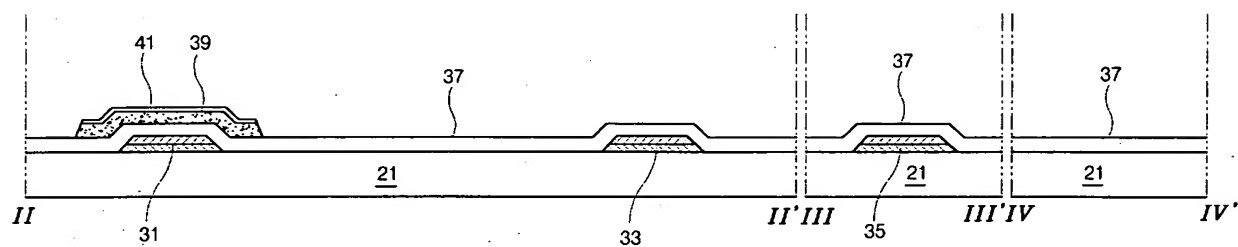
[Fig. 2d]



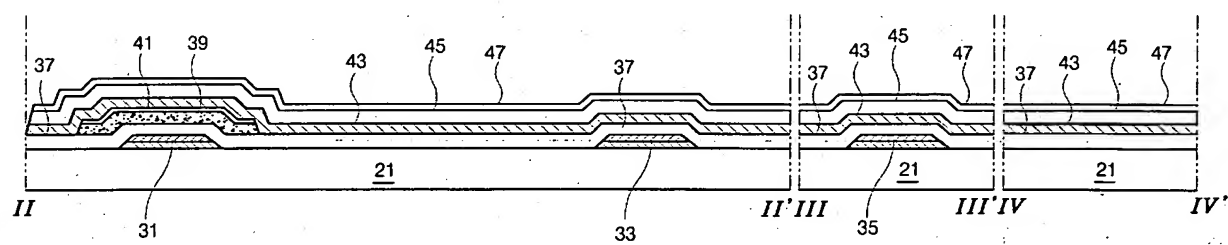
[Fig. 2e]



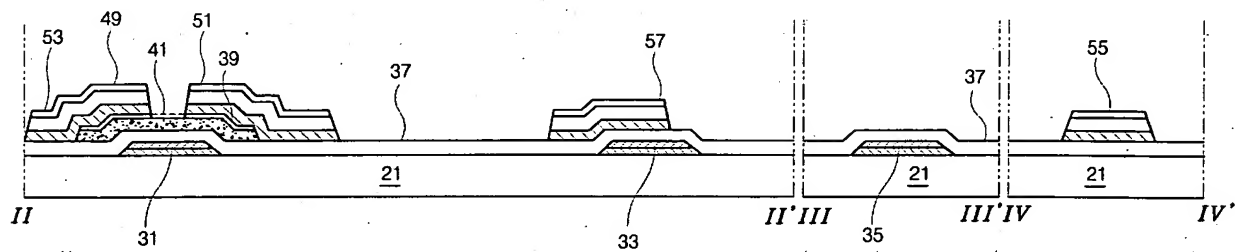
[Fig. 3a]



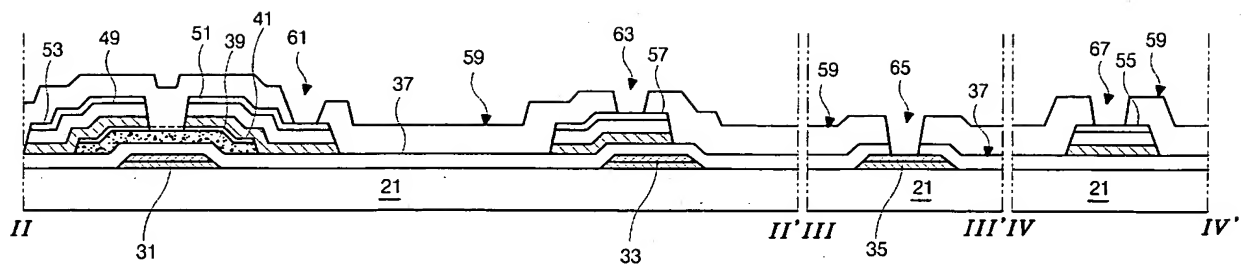
[Fig. 3b]



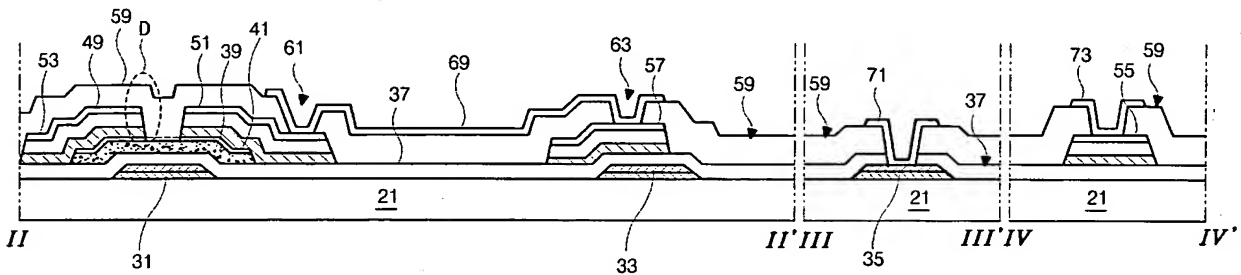
[Fig. 3c]



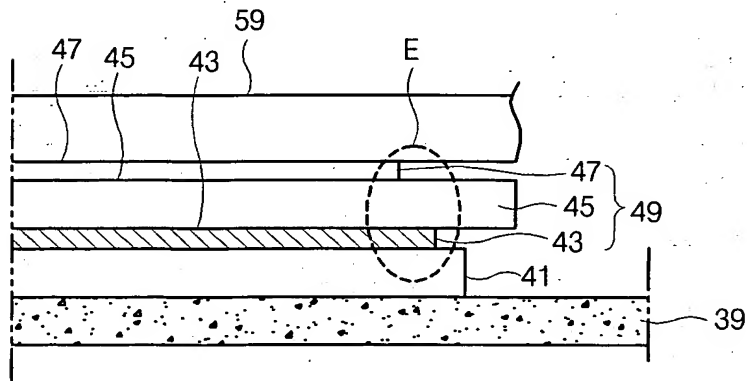
[Fig. 3d]



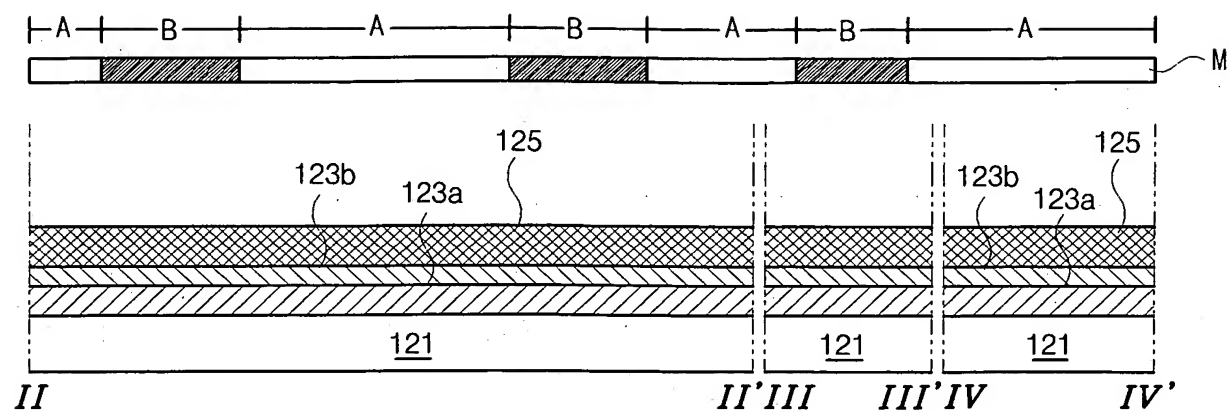
[Fig. 3e]



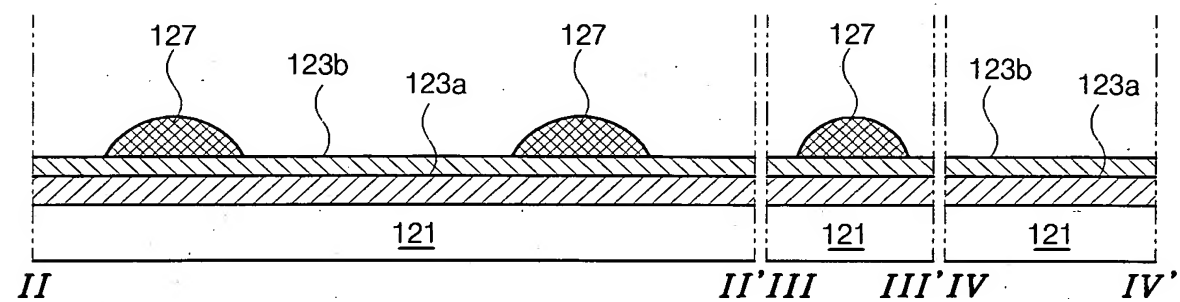
[Fig. 4]



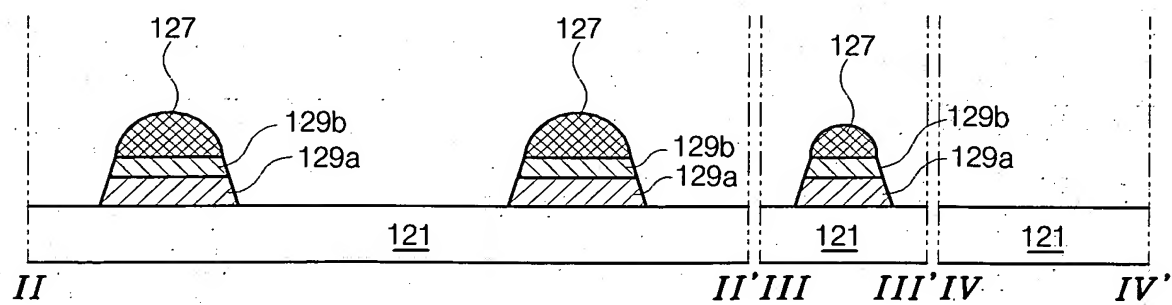
[Fig. 5a]



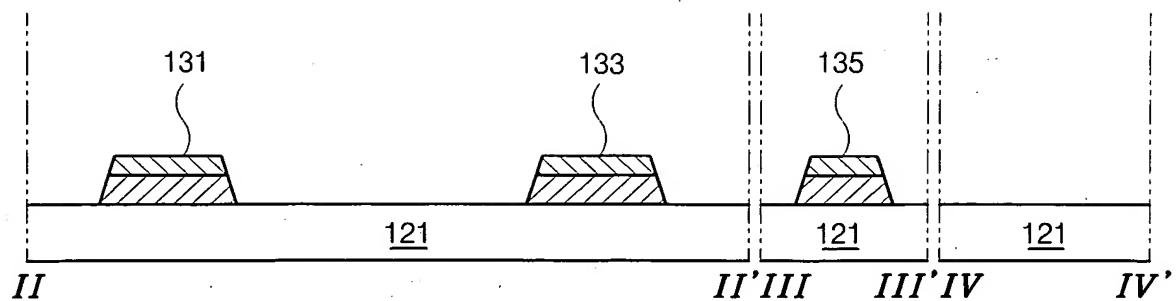
[Fig. 5b]



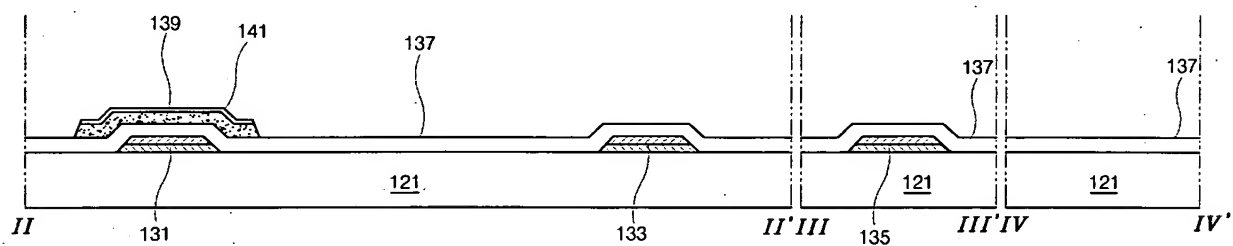
[Fig. 5c]



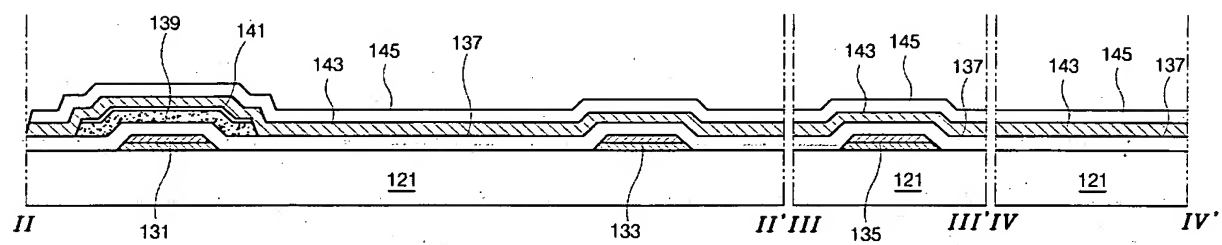
[Fig. 5d]



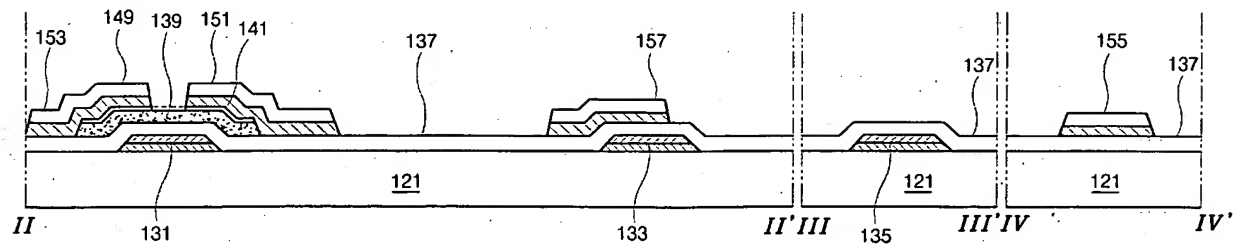
[Fig. 6a]



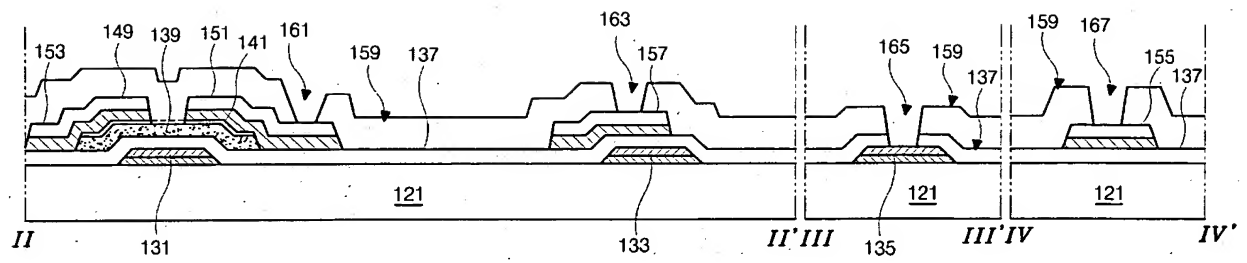
[Fig. 6b]



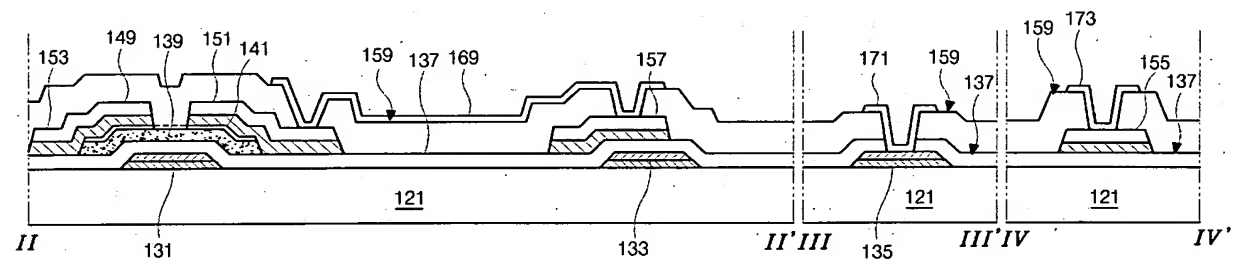
[Fig. 6c]



[Fig. 6d]



[Fig. 6e]



[Fig. 7]

